FIG. 1

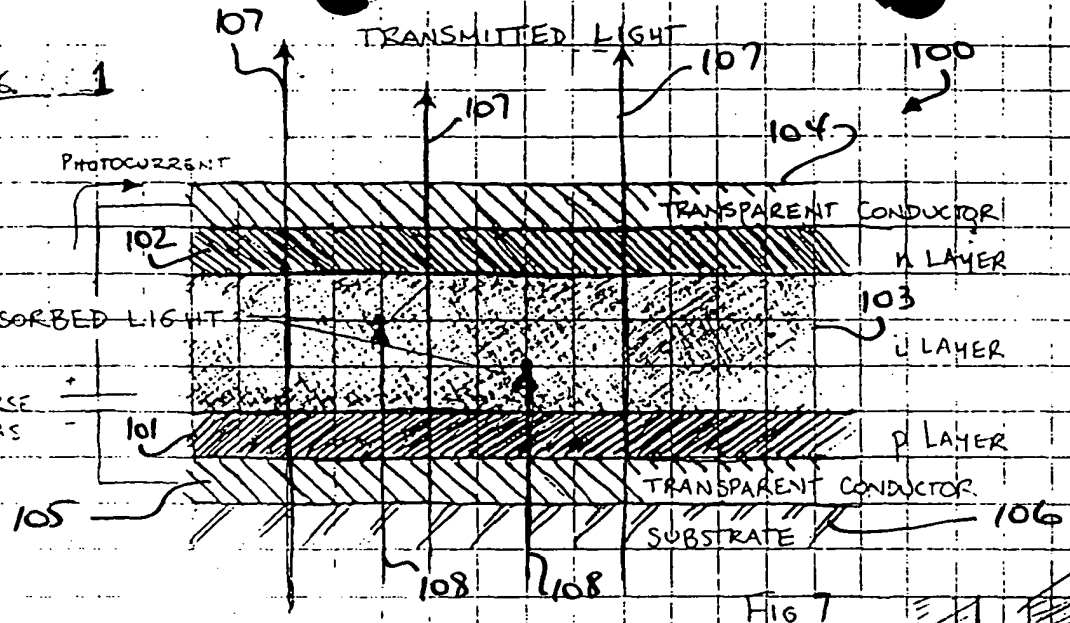


FIG 4

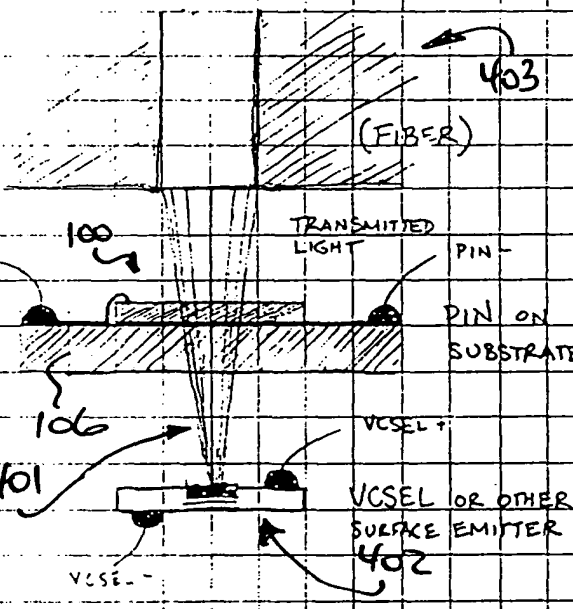


FIG 7

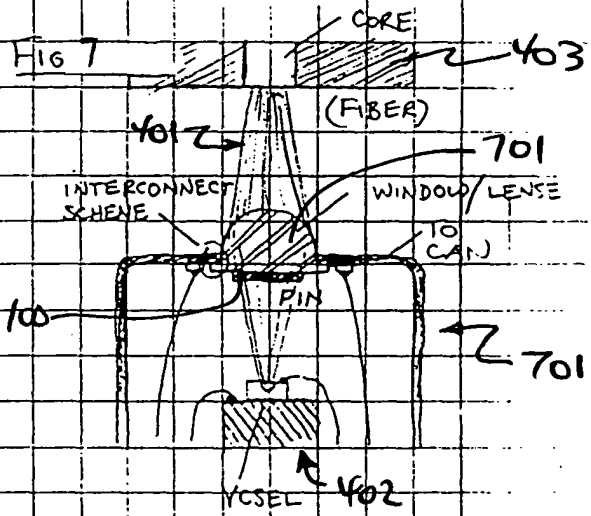


FIG 5

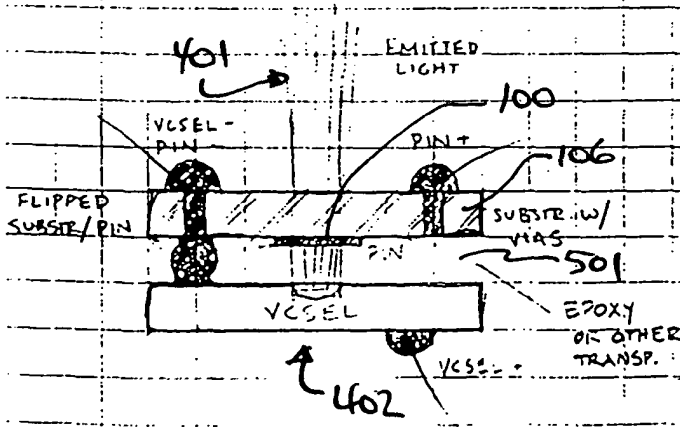
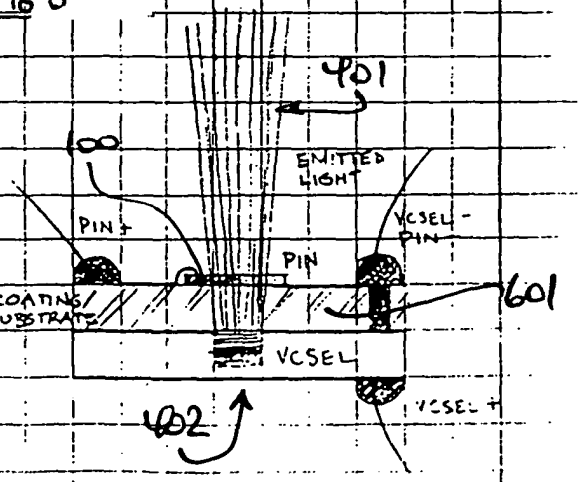


FIG 6



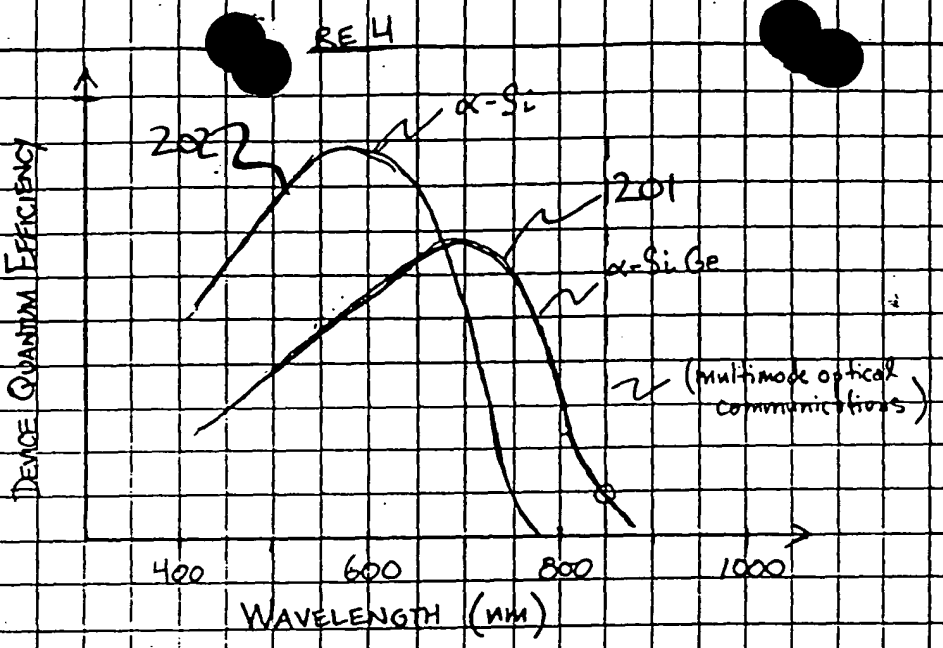

RE 4
DEVICE QUANTUM EFFICIENCY
202
α-Si
201
α-SiGe
(multimode optical communications)
400
600
800
1000
WAVELENGTH (nm)

Fig. 2.

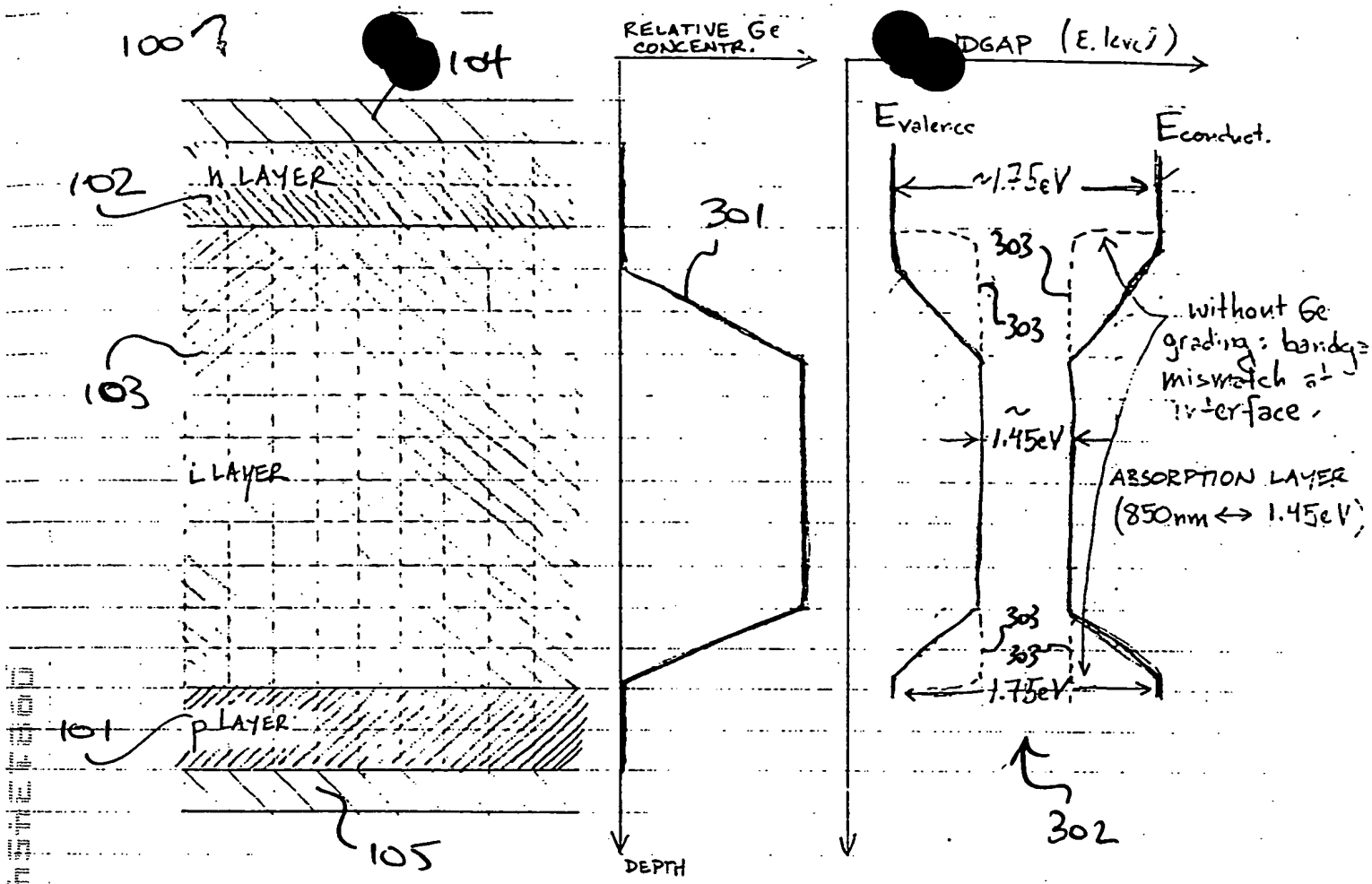

100
104
102
n LAYER
103
i LAYER
101
p LAYER
105
RELATIVE Ge CONCENTR.
DEPTH
301
BANDGAP (E. level)
E valence
E conduct.
~1.75eV
303
303
without Ge grading: bandgap mismatch at interface.
~1.45eV
ABSORPTION LAYER (850nm ↔ 1.45eV)
303
303
1.75eV
302

Fig. 3

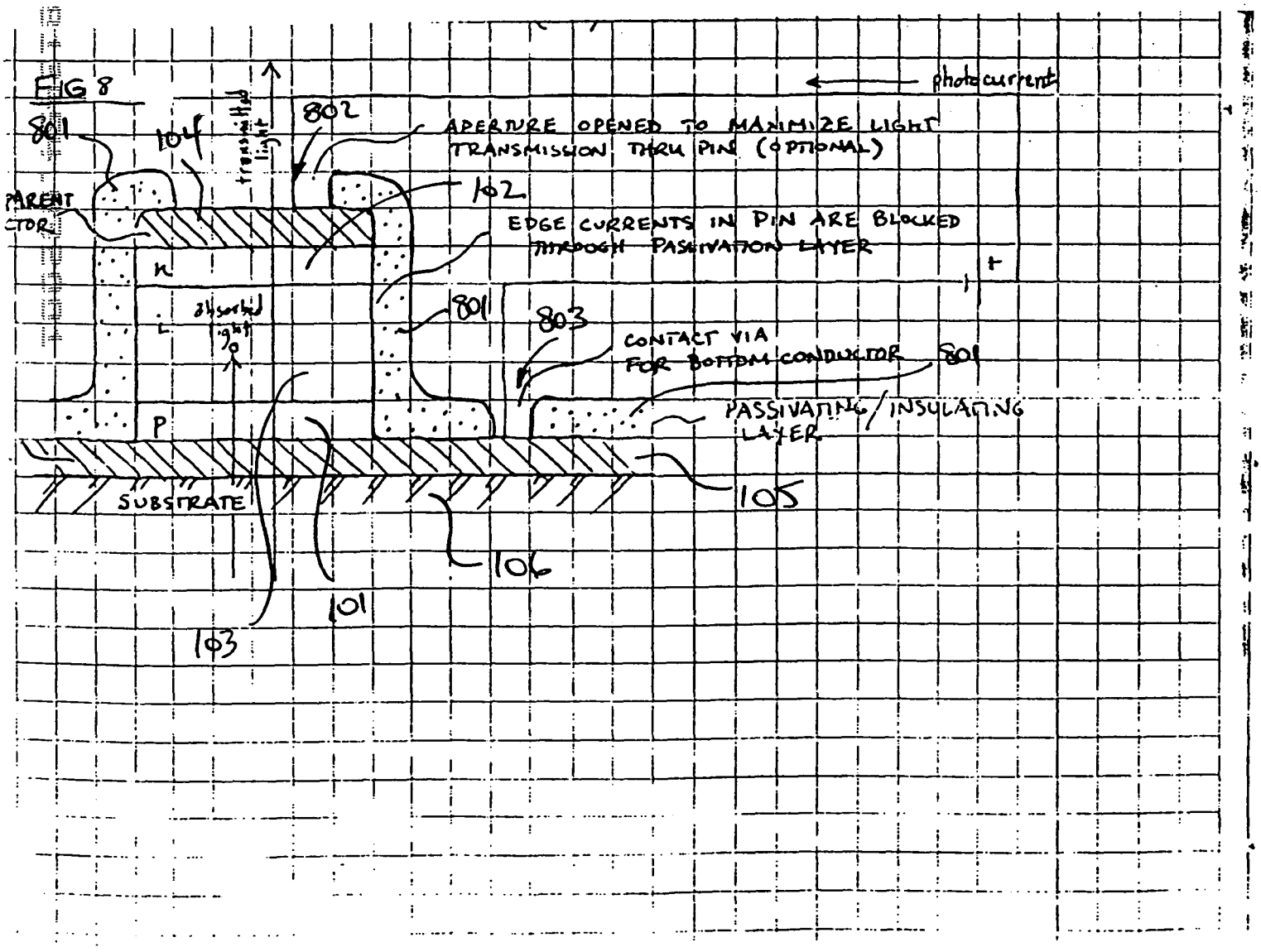


FIG 8
801
104
transmitted light
802
APERTURE OPENED TO MAXIMIZE LIGHT TRANSMISSION THRU PIN (OPTIONAL)
PARENT CTOR
102
EDGE CURRENTS IN PIN ARE BLOCKED THROUGH PASSIVATION LAYER
N
absorbed light
801
803
CONTACT VIA FOR BOTTOM CONDUCTOR
801
P
PASSIVATING / INSULATING LAYER
SUBSTRATE
105
106
101
103
photocurrent

FIG 9

MOST SIMPLE STRUCTURE
- DON'T PATTERN BOTTOM T.C.
- USE TOP T.C. AS PIN ETCH MASK

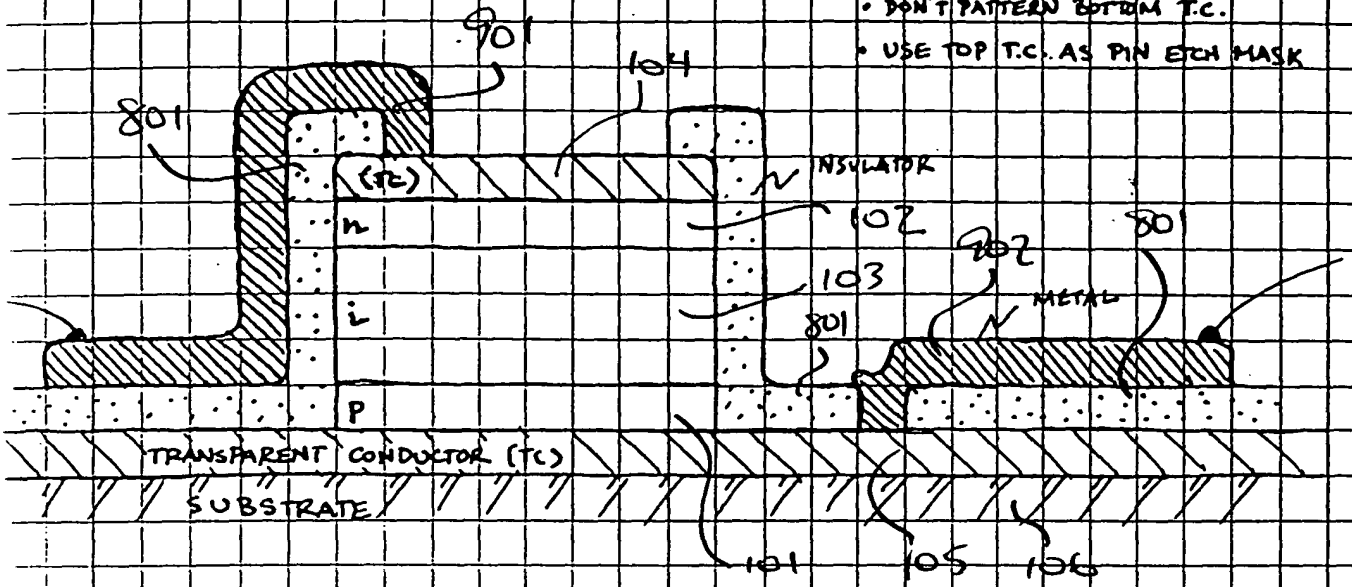


FIG 10

ADD TOP T.C. AFTER INSULATOR; SLIGHTLY LARGER APERTURE

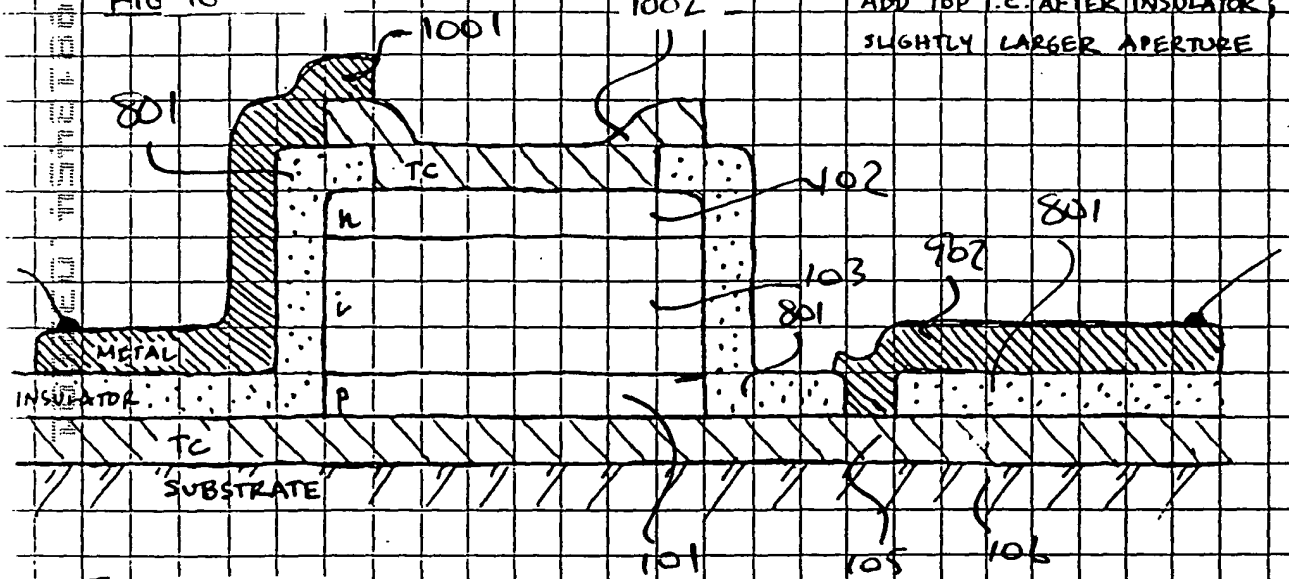


FIG 11

PATTERN BOTTOM T.C. — REDUCE CAPACITANCES

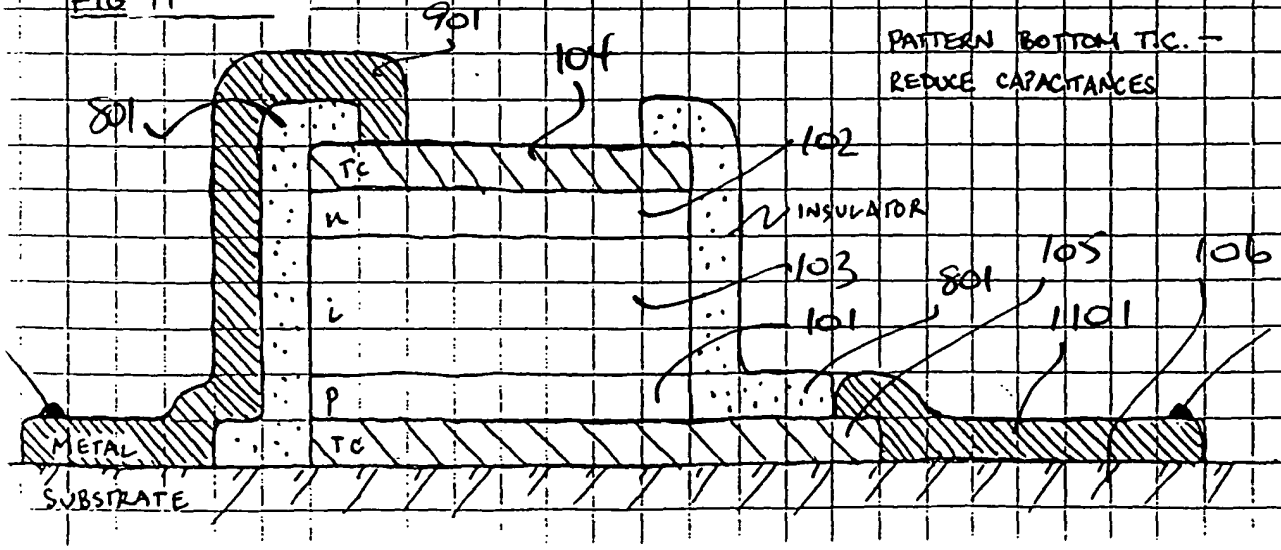


FIG. 12

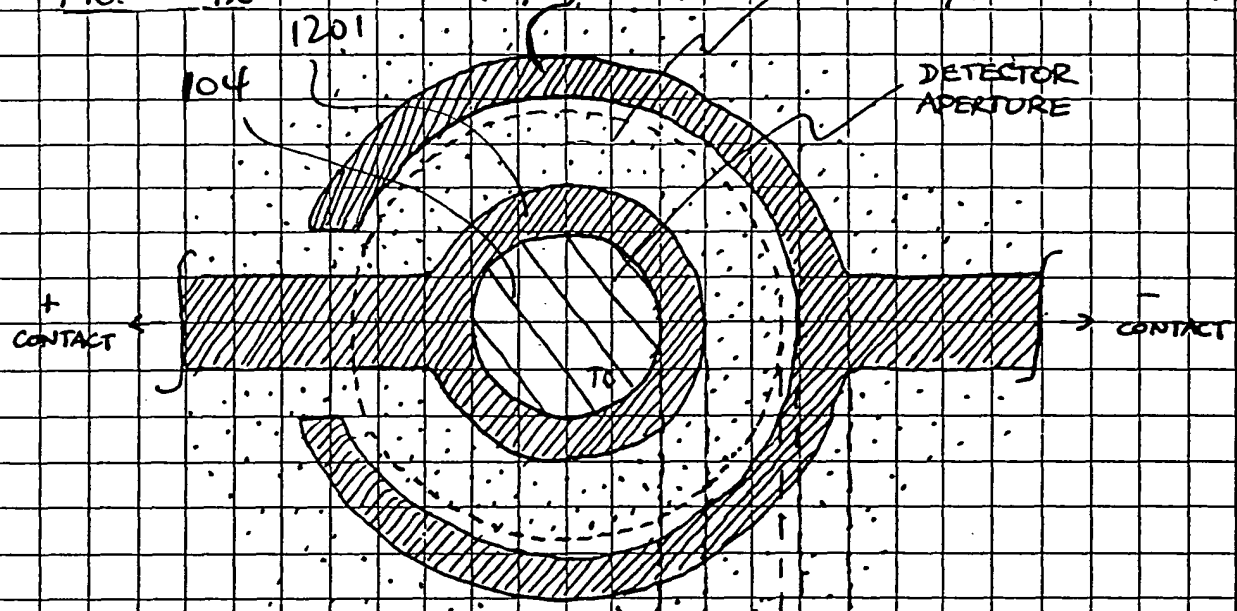
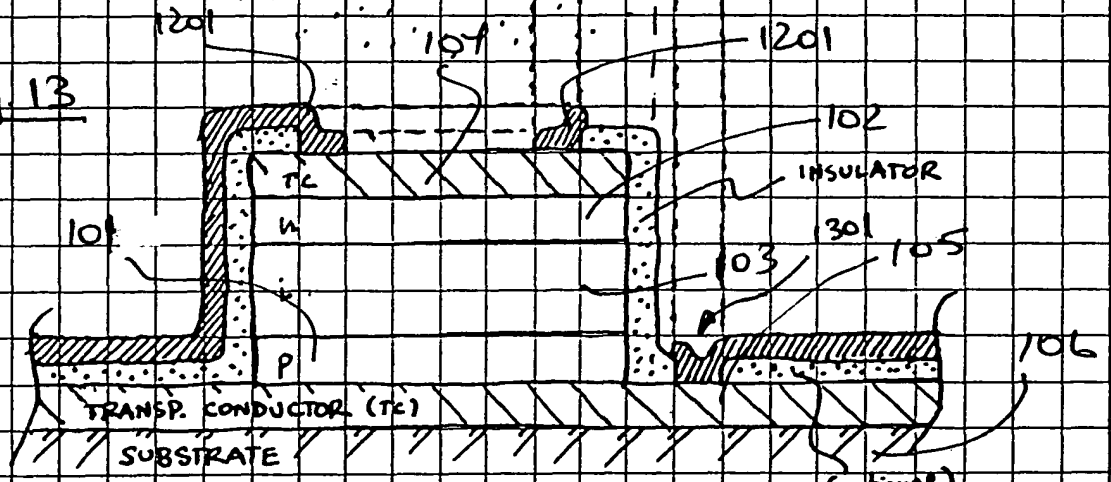


Fig. 13



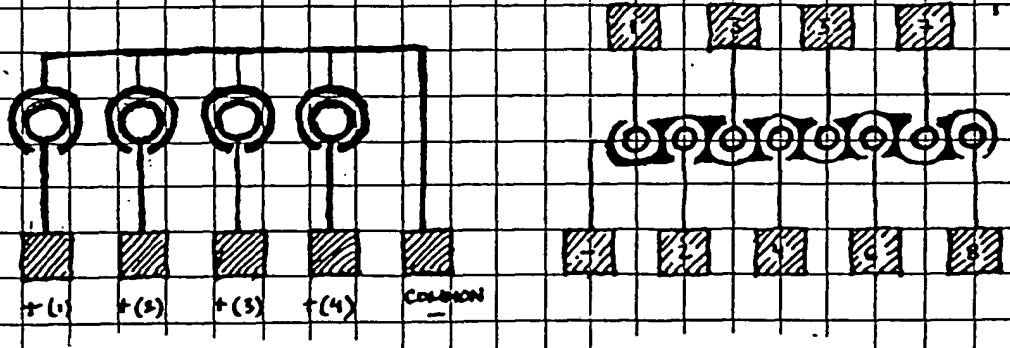
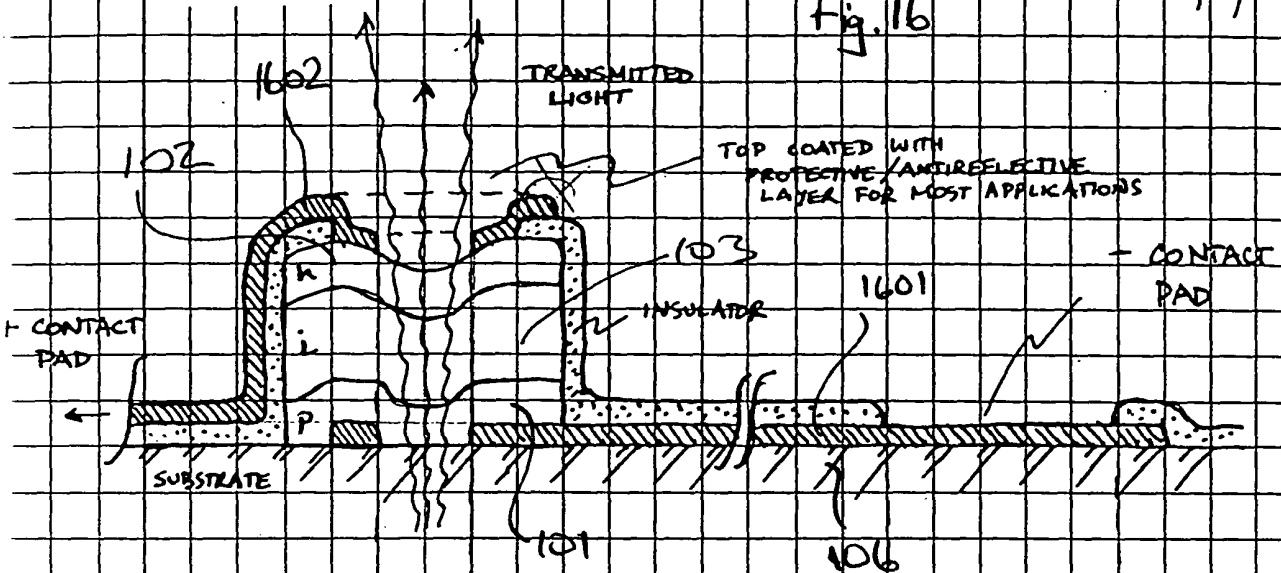


Fig. 14

Fig. 15

3/25/00

Fig. 16



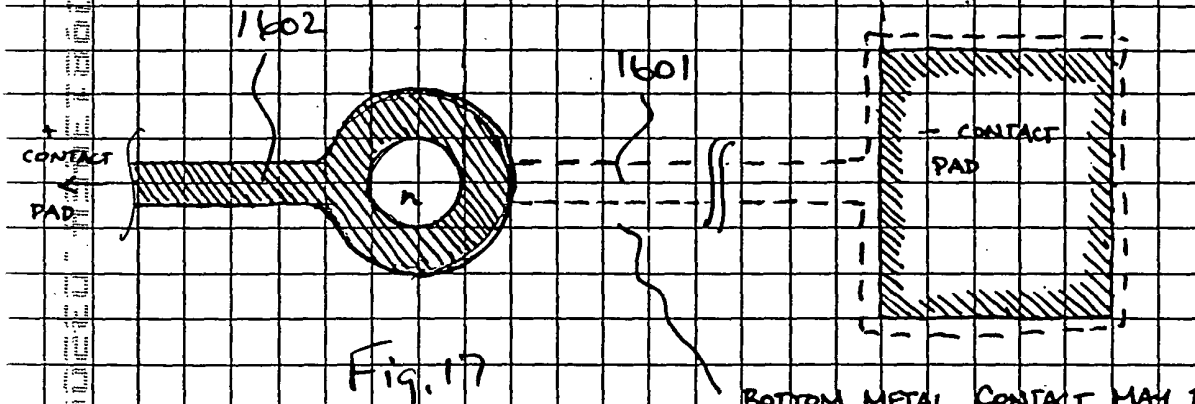


Fig. 17

5/3/00

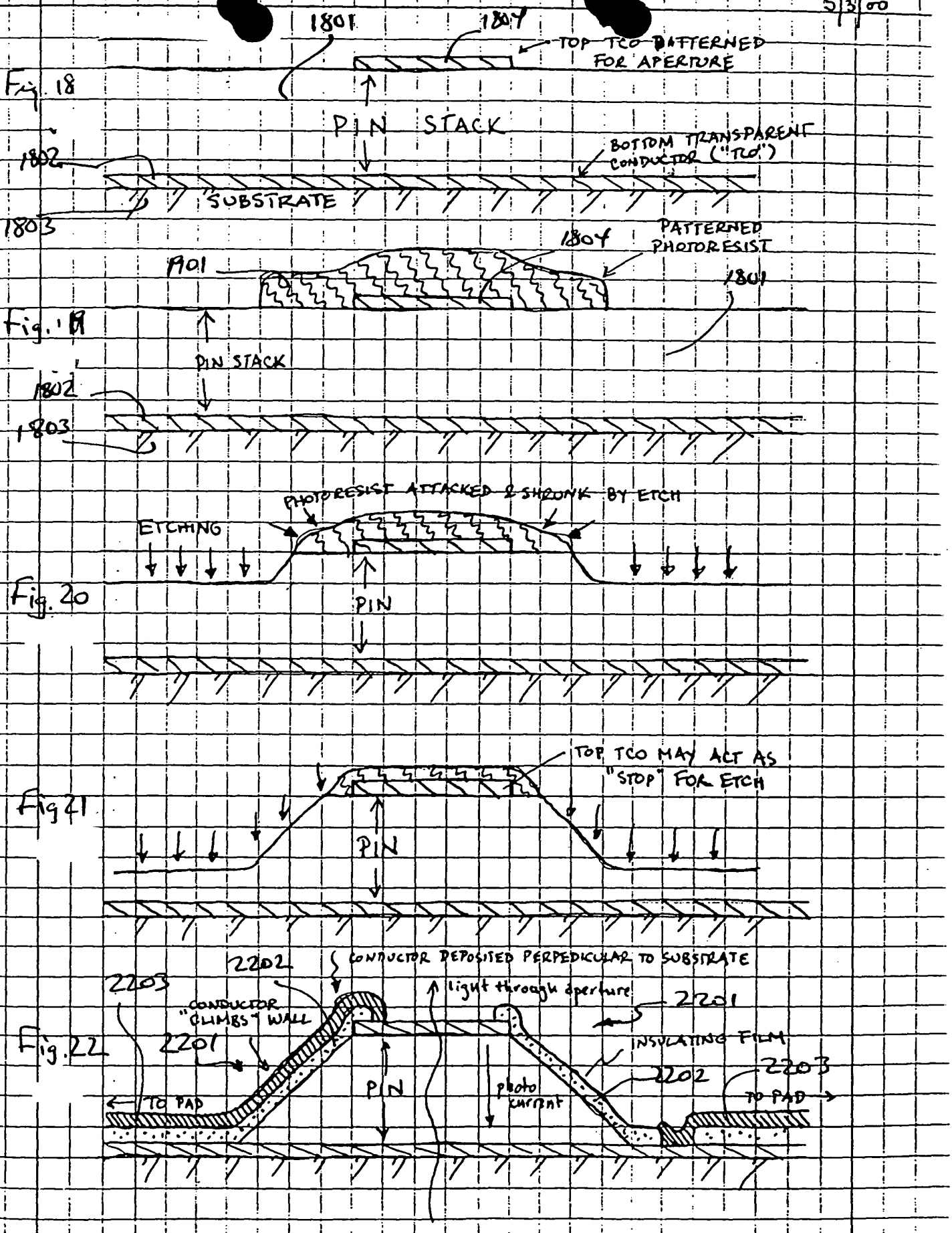


Fig. 18

Fig. 19

Fig. 20

Fig 21

Fig. 22

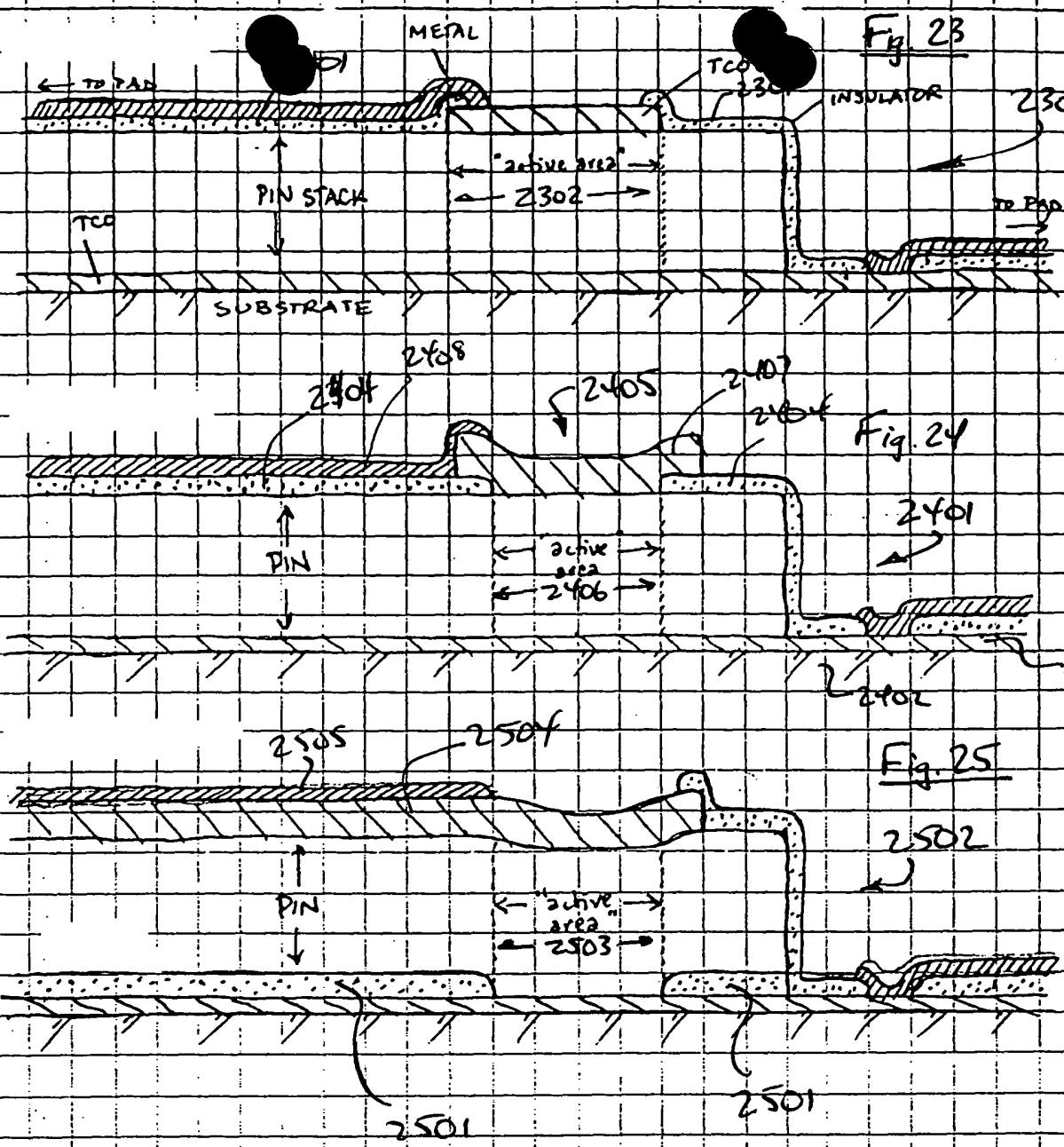


Fig 23
METAL
TO PAD
TCO
2304
INSULATOR
2303
"active area"
2302
PIN STACK
TCO
TO PAD
SUBSTRATE
2408
2401
2405
2407
2404
Fig. 24
2401
PIN
active area
2406
2403
2402
2505
2504
Fig. 25
2502
PIN
active area
2503
2501
2501

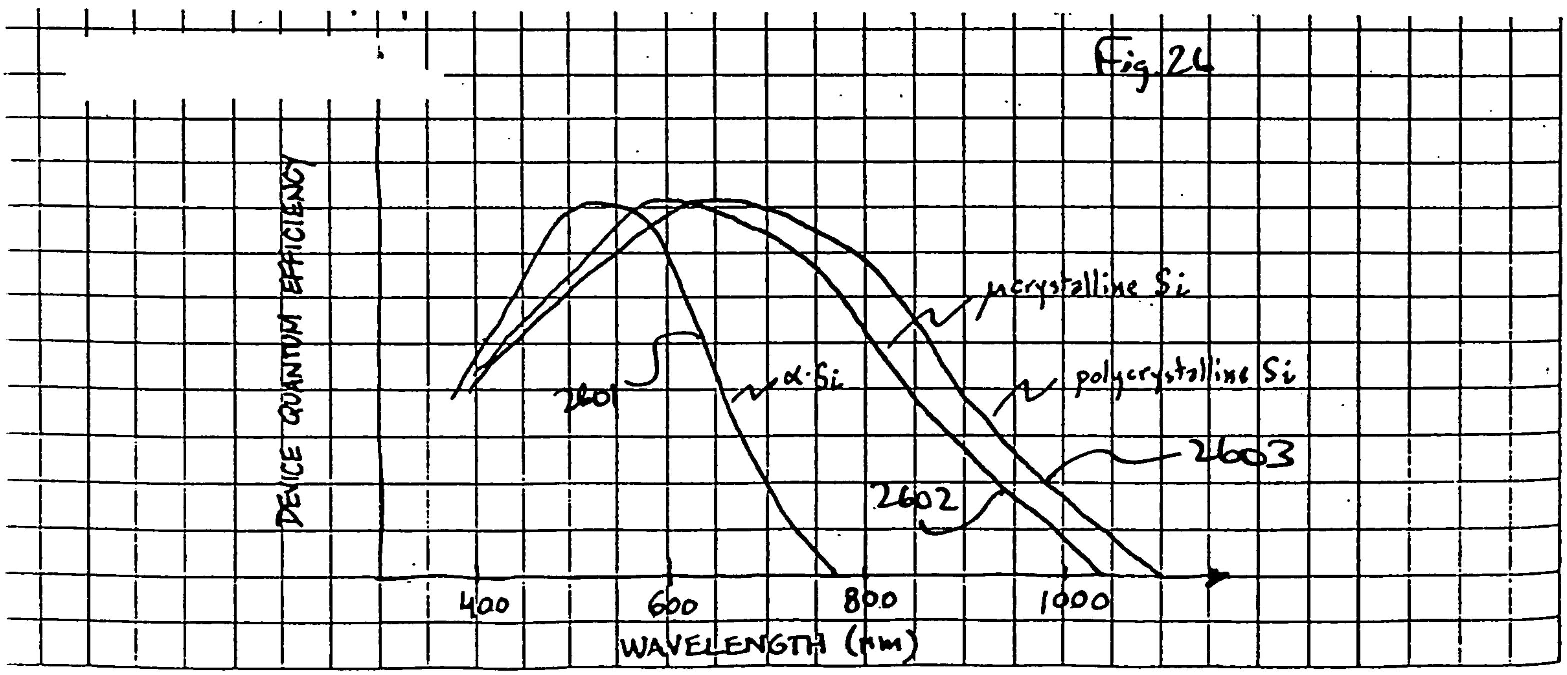

DEVICE QUANTUM EFFICIENCY
WAVELENGTH (nm)
400
600
800
1000
2601
α-Si
μcrystalline Si
polycrystalline Si
2602
2603

Fig. 26

Fig. 27

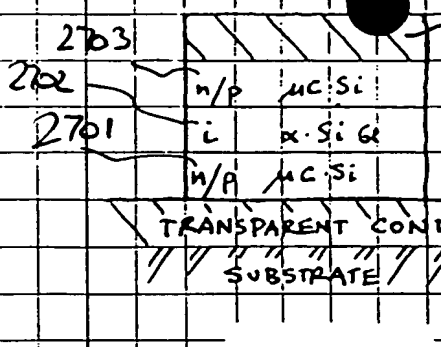


Fig. 28

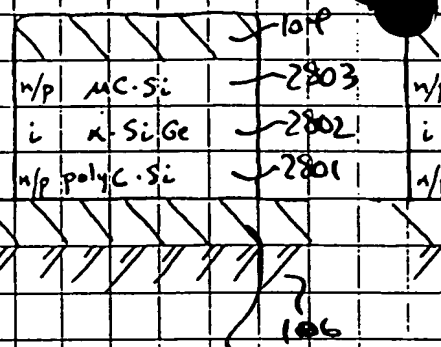
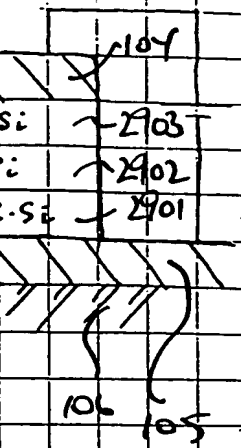


Fig. 29



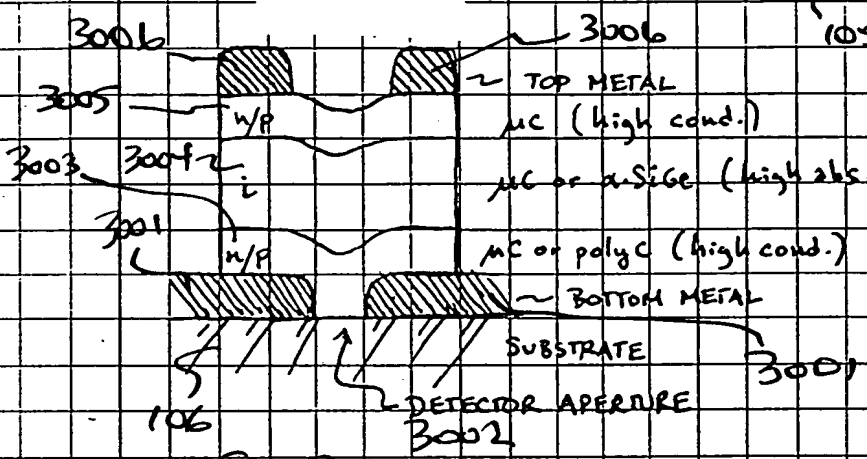


Fig. 30

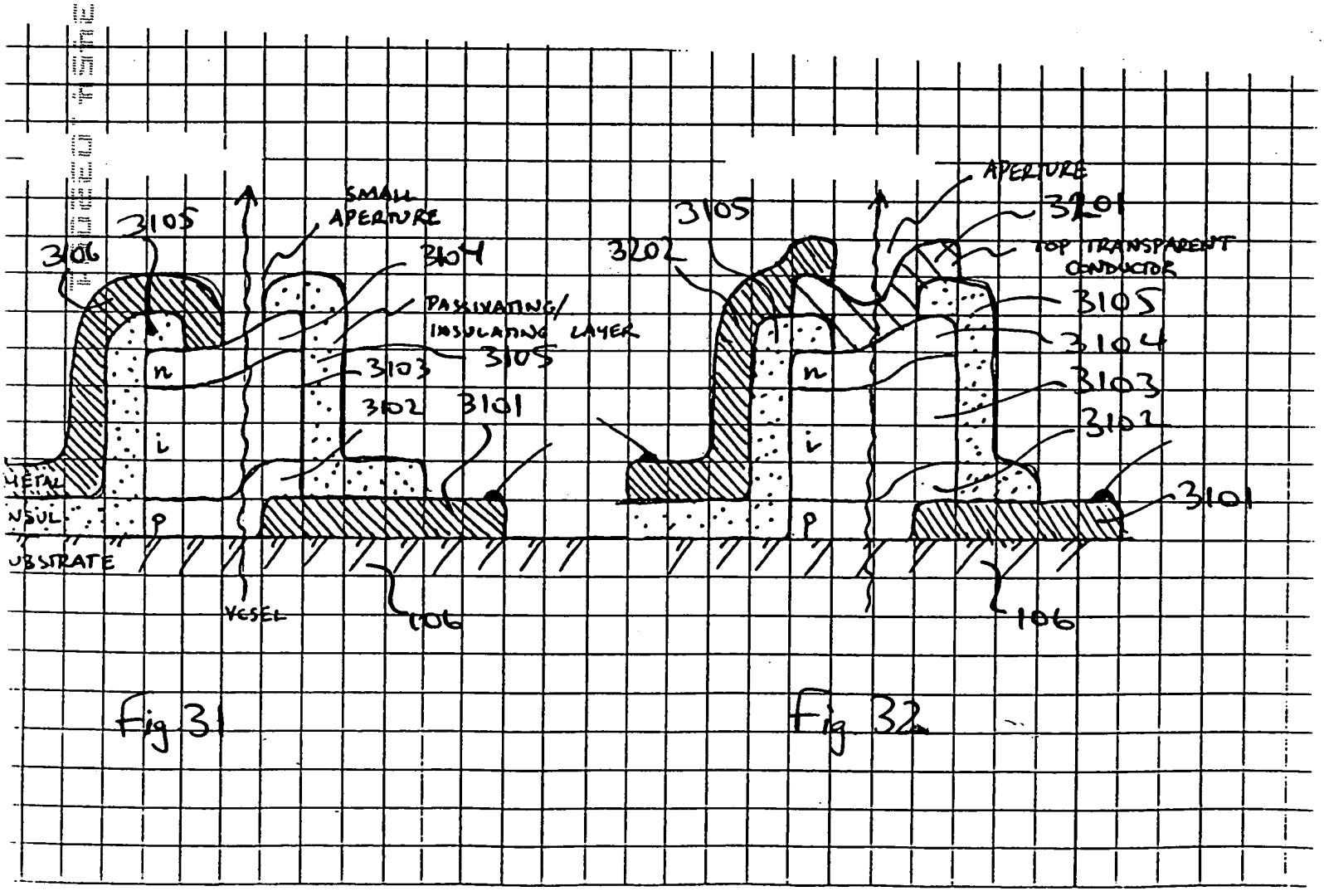

3105
3106
SMALL APERTURE
3104
PASSIVATING/ INSULATING LAYER
3103
3102
3101
n
i
p
METAL
INSUL
SUBSTRATE
VESEL
106
3105
3102
APERTURE
3101
TOP TRANSPARENT CONDUCTOR
3105
3104
3103
3102
3101
106

Fig 31

Fig 32

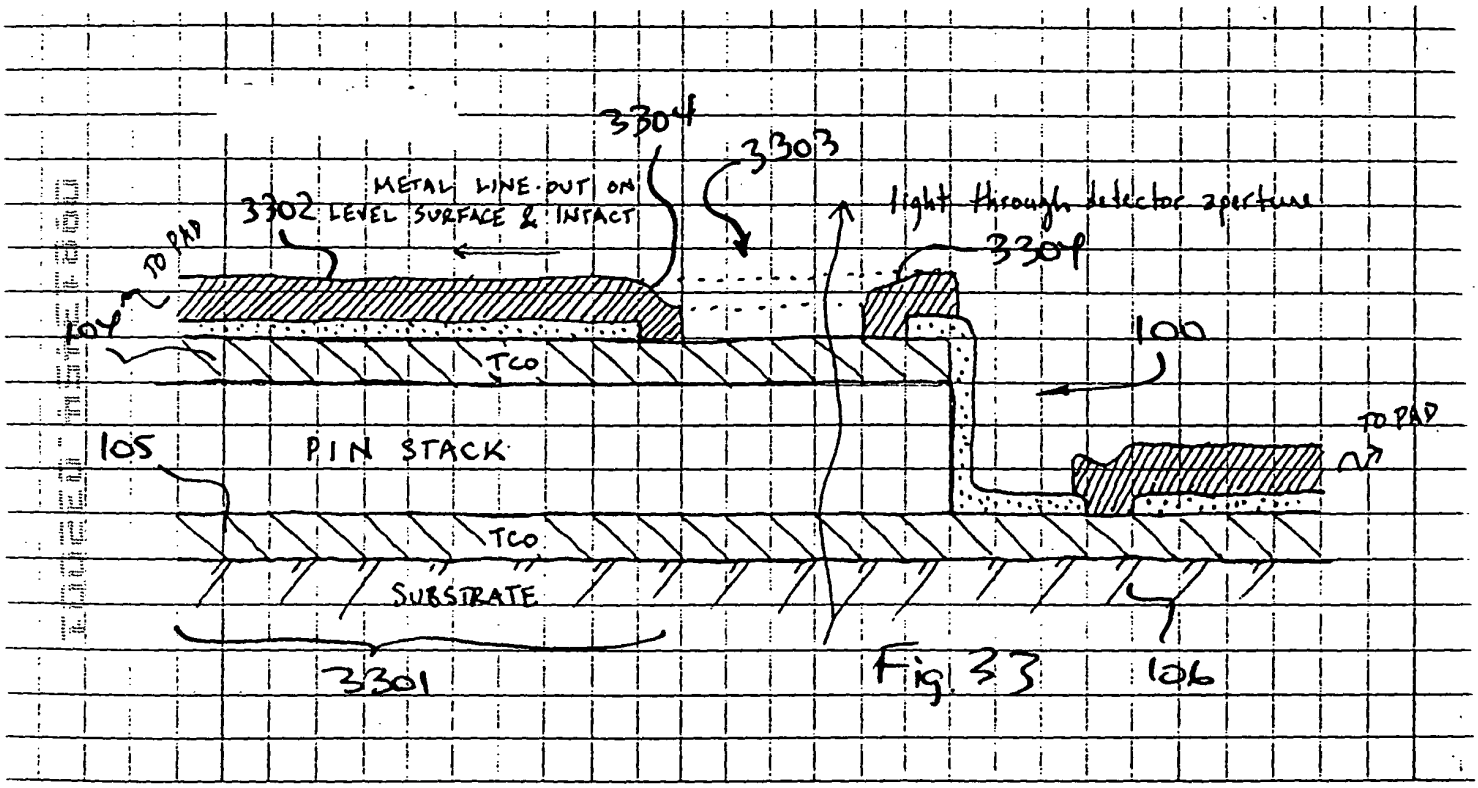
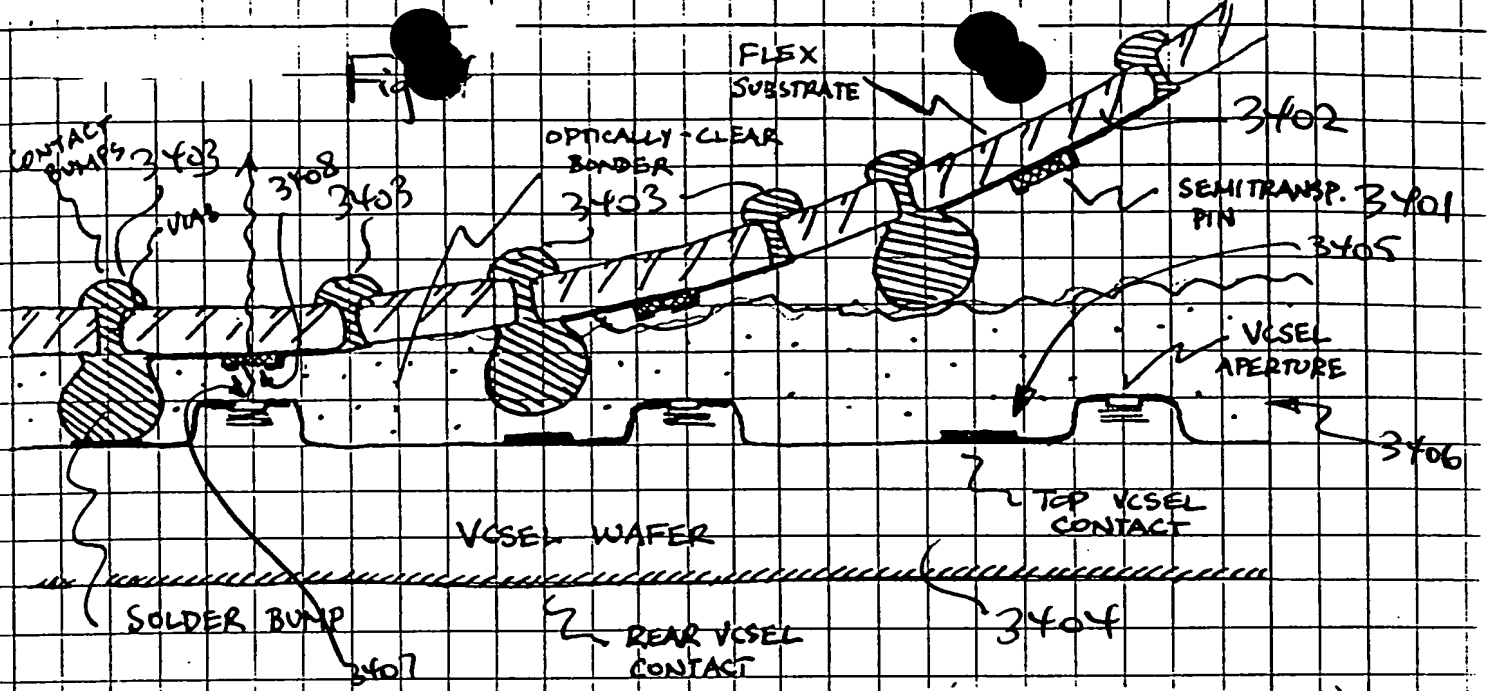

3304
3303
METAL LINE OUT ON LEVEL SURFACE & INTACT
3302
light through detector aperture
TO PAD
3301
TCO
100
PIN STACK
105
TCO
SUBSTRATE
TO PAD
3301
106

Fig 33



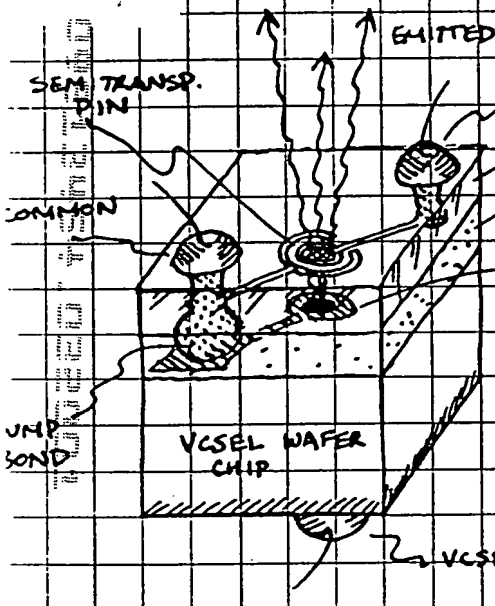


Fig 34

NOTE: ALTERNATIVE CONFIGURATION HAS 3 TOP CONTACTS (NO COMMON); MAY BE PREFERABLE FOR HIGH-SPD. SWITCHING. (PERHAPS EVEN FORM HOLE THROUGH PIN SUBSTRATE & BOND LAYER TO VCSEL TOP CONTACT).

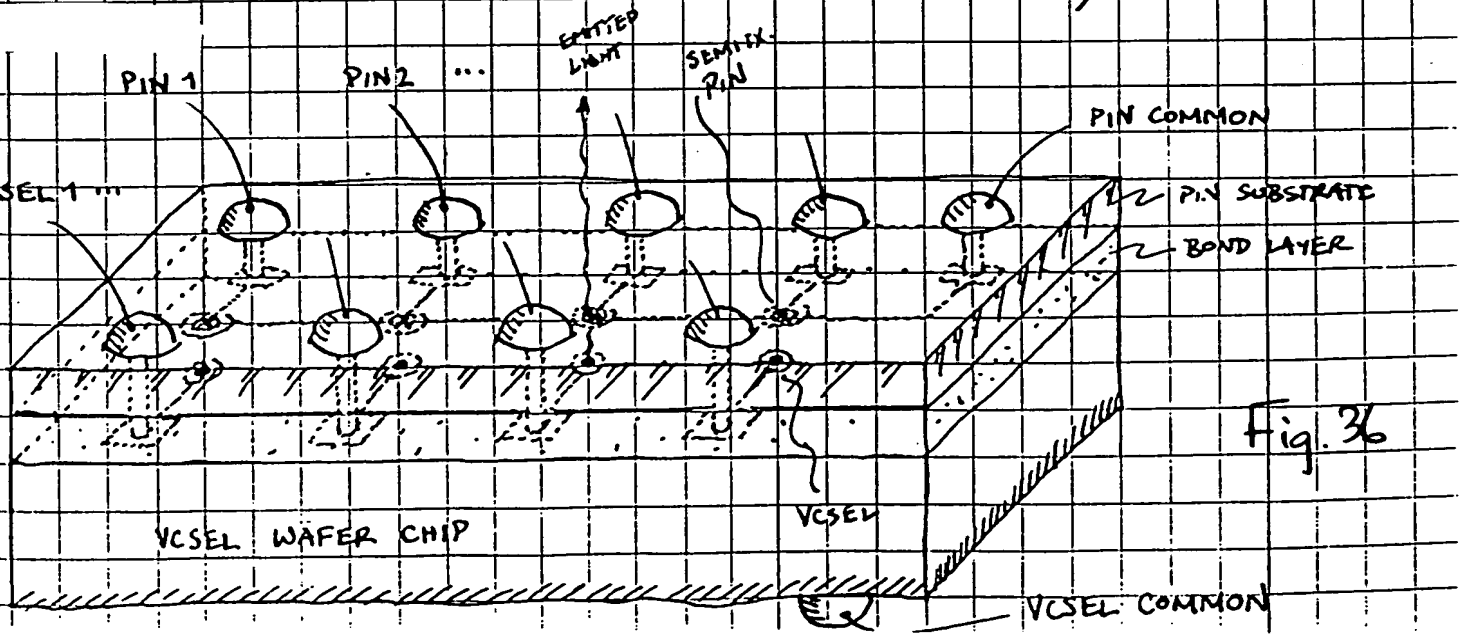


Fig. 36

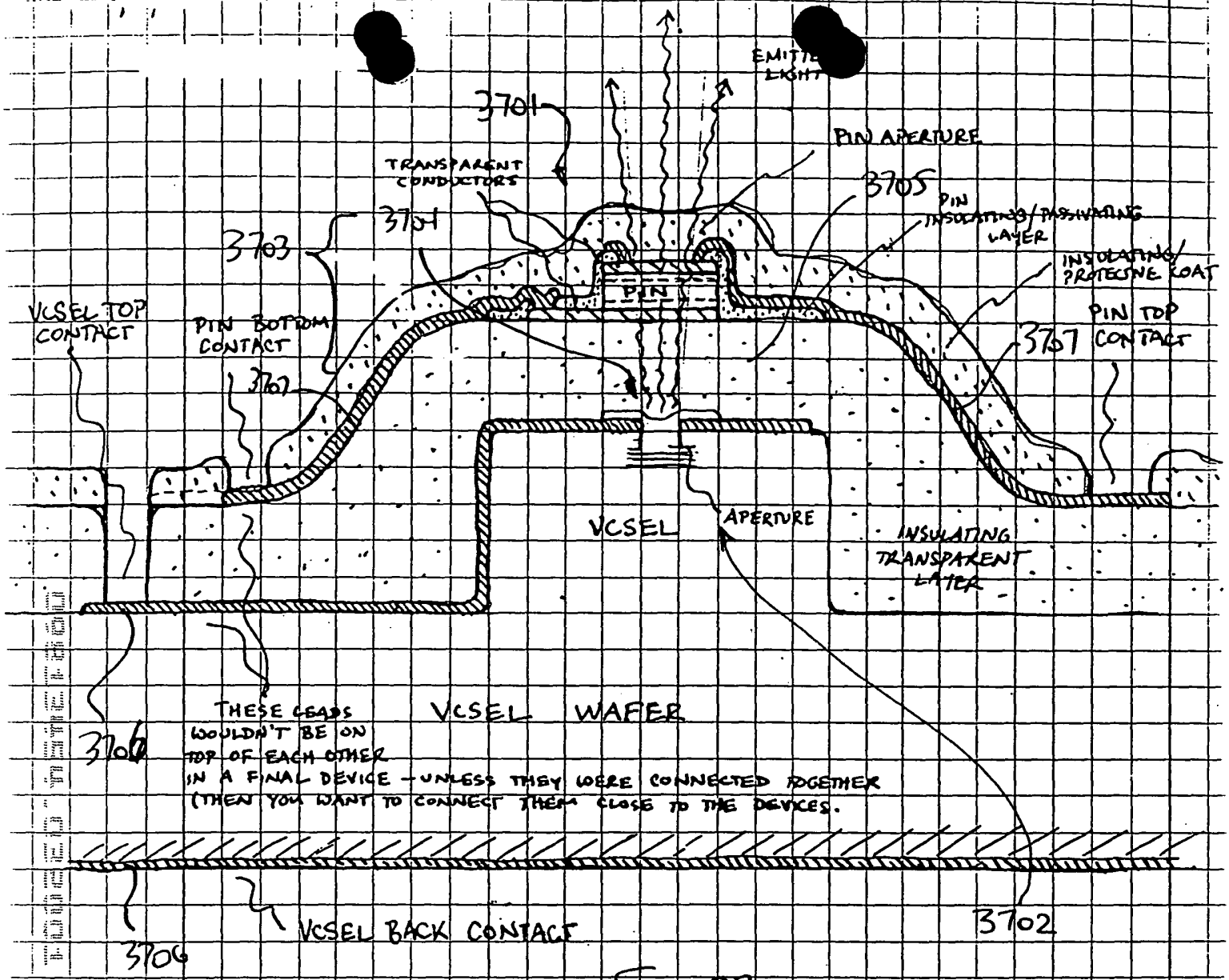

EMITTED LIGHT
3701
PIN APERTURE
TRANSPARENT CONDUCTORS
3705
3704
PIN INSULATING/PASSIVATING LAYER
3703
INSULATING/PROTECTIVE COAT
PIN
VCSEL TOP CONTACT
PIN BOTTOM CONTACT
PIN TOP CONTACT
3707
3702
VCSEL APERTURE
INSULATING TRANSPARENT LAYER
THESE LEADS WOULDN'T BE ON TOP OF EACH OTHER IN A FINAL DEVICE - UNLESS THEY WERE CONNECTED TOGETHER (THEN YOU WANT TO CONNECT THEM CLOSE TO THE DEVICES.
VCSEL WAFER
3706
VCSEL BACK CONTACT
3706

Fig. 37

3/28/00

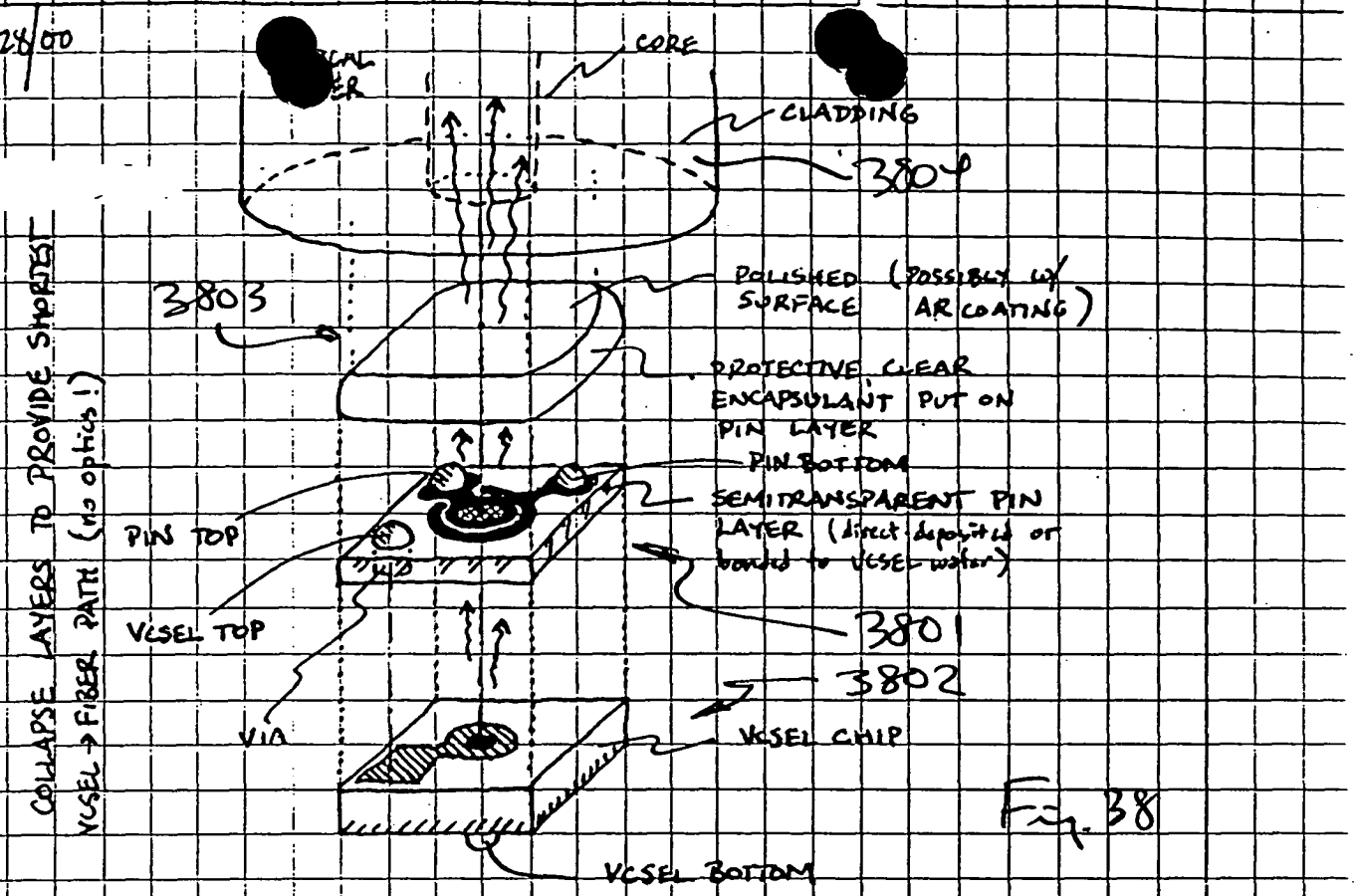


Fig. 38

.. SUCH A PACKAGE WOULD ALLOW LOW-COST, DIRECT COUPLING IN A FIBER CONNECTOR (VCSEL APERTURE ≤ 25 μm AND MULTIMODE FIBER CORE ≥ 50-625 μm; VCSEL BEAM DIVERGENCE ≤ 20°, AND PIN LAYER IS THIN).

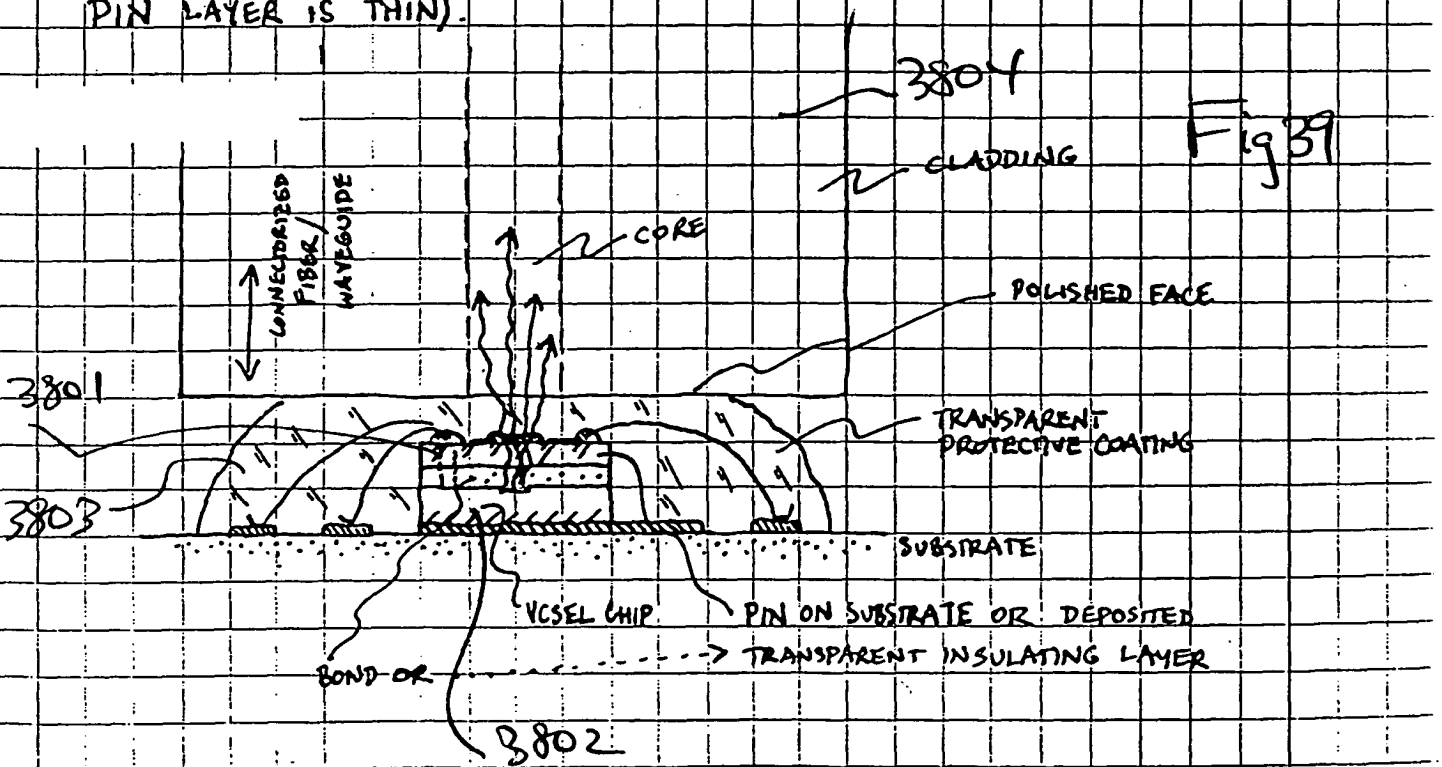
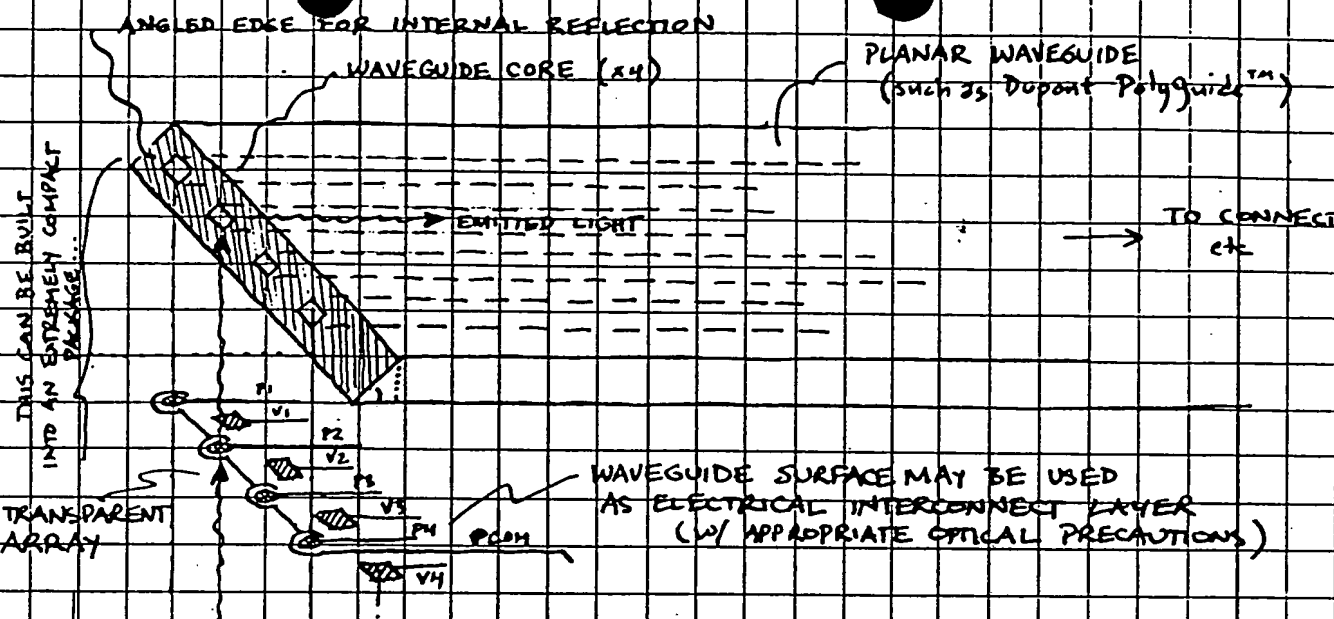
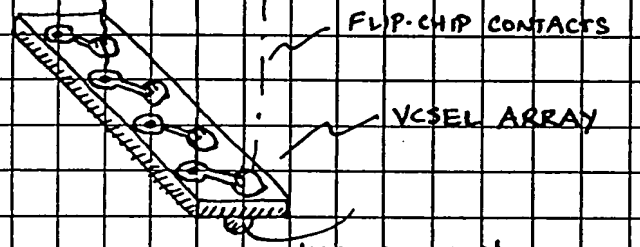


Fig 39

3/28/00

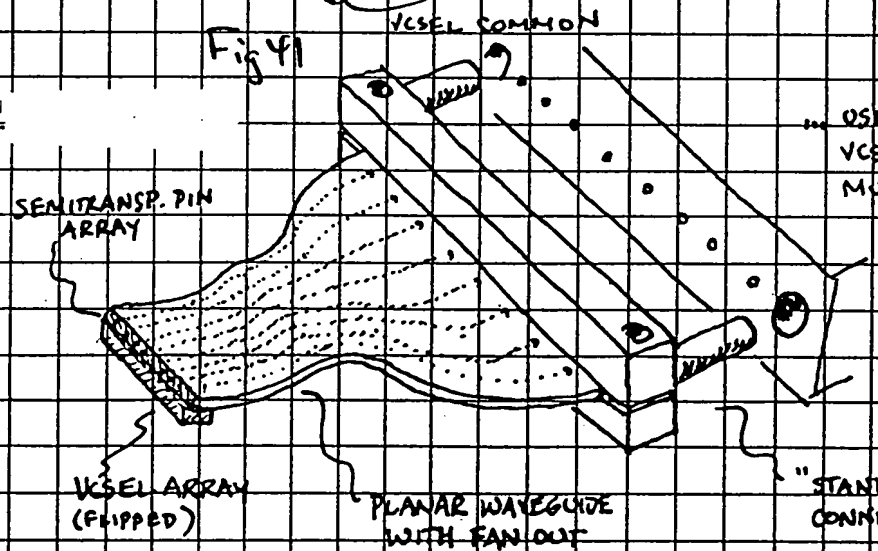
Fig. 40





PIN ARRAY IS:
(1) PATTERNED ON WAVEGD.
(2) PATTERNED ON VCSEL CHIP
OR (3) PATTERNED ON SEPERATE SUBSTRATE

Fig 41



... USE VERY SMALL INTEGRAL VCSEL ARRAY TO ADDRESS MULTIPLE FIBERS / STANDARD CONNECTORS.

Fig. 42